

CLAIMS

What is claimed is:

- 1 1. A method of managing power in a graphics controller, comprising:
2 Receiving a change indication related to a system power supply;
3 Adjusting a first clock; and
4 Adjusting a controller power supply voltage.

- 1 2. The method of claim 1 further comprising:
2 Signaling a BIOS with an indication of a change related to the system
3 power supply.

- 1 3. The method of claim 2 further comprising:
2 Receiving a set of one or more available clock rates;
3 Checking a state of the graphics controller;
4 Choosing a desired clock rate from the set of available clock rates;
5 Adjusting a second clock to conform to the desired clock rate; and
6 wherein:
7 Adjusting the first clock comprises reducing a rate of the first clock; and
8 Adjusting the controller power supply voltage comprises reducing the
9 controller power supply voltage.

1 4. The method of claim 3 further comprising:

2 Disabling a CLUT.

1 5. The method of claim 4 wherein:

2 Disabling the CLUT responsive to checking the state of the graphics

3 controller.

1 6. The method of claim 5 further comprising:

2 Notifying a system to reduce brightness of a display.

1 7. The method of claim 6 wherein:

2 Notifying the system comprises notifying a chipset directly.

1 8. The method of claim 1 wherein:

2 The controller power supply voltage is associated with a controller power

3 supply internal to the graphics controller.

1 9. The method of claim 2 wherein:

2 The controller power supply voltage is associated with a controller power

3 supply external to the graphics controller, and adjusting the controller power

4 supply voltage includes programming the controller power supply with a signal.

1 10. The method of claim 1 wherein:
2 Adjusting the first clock comprises increasing a rate of the first clock; and
3 Adjusting the controller power supply voltage comprises increasing the
4 controller power supply voltage.

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1 11. The method of claim 10 further comprising:
2 Increasing a clock rate of a second clock.

1 12. The method of claim 11 further comprising:
2 Enabling a CLUT.

1 13. The method of claim 1 further comprising:
2 Detecting a change related to a system power supply.

1 14. The method of claim 13 further comprising:
2 Installing a software routine in a system containing the graphics controller,
3 the software routine suitable for detecting the change related to the system
4 power supply.

1 15. A method of effecting power management of a graphics controller in
2 an operating system comprising:

3 Detecting a change in a system power supply;
4 Notifying the graphics controller of the change;
5 Receiving an indication of power reduction in the graphics controller; and
6 Providing a set of available clock frequencies to the graphics controller.

1 16. The method of claim 15 further comprising:

2 Receiving a signal from the graphics controller to reduce brightness of a
3 display.

1 17. The method of claim 16 further comprising:

2 Reducing brightness of the display.

1 18. The method of claim 17 further comprising:

2 Receiving a software routine suitable for notifying the graphics controller;

3 and wherein:

4 Notifying the graphics controller comprises executing the software routine.

1 19. The method of claim 18 further comprising:

2 Programming the set of available clock frequencies.

1 20. The method of claim 3 further comprising:
2 Disabling a first portion of circuitry of the graphics controller.

1 21. The method of claim 20 wherein
2 Disabling the first portion of circuitry responsive to checking the state of
3 the graphics controller.

1 22. The method of claim 21 further comprising:
2 Enabling the first portion of circuitry of the graphics controller.

1 23. A graphics controller comprising:
2 A power supply input configured to receive power at a range of voltages;
3 A power supply control output;
4 A first clock;
5 And
6 A system power supply change input.

1 24. The graphics controller of claim 23 further comprising:
2 A first clock control output.

1 25. The graphics controller of claim 24 further comprising:

2 A memory coupled to the first clock.

1 26. The graphics controller of claim 24 further comprising:

2 A second clock; and

3 A second clock control output.

1 27. The graphics controller of claim 26 further comprising:

2 A memory coupled to the first clock.

1 28. The graphics controller of claim 27 wherein:

2 The memory is integrated with other portions of the graphics controller on
3 a single substrate.

1 29. The graphics controller of claim 27 further comprising:

2 A voltage regulator coupled to the power supply input and the power
3 supply control output.

1 30. The graphics controller of claim 29 wherein:

2 The voltage regulator is integrated with other portions of the graphics
3 controller on a single substrate.

1 31. The graphics controller of claim 30 further comprising:

2 A VGA BIOS.

1 32. The graphics controller of claim 26 further comprising:

2 A brightness output configured to signal to a system that a reduction in

3 brightness of a display is appropriate.

1 33. The graphics controller of claim 32 wherein:

2 The brightness output is suitable for coupling directly to a video control

3 chipset.

1 34. The graphics controller of claim 32 further comprising:
2 A 2D engine;
3 A 3D engine;
4 A CLUT coupled to the 3D engine and coupled to the 2D engine;
5 A system interface including the system power supply input;
6 A video interface including the second clock and the second clock control
7 output;
8 A power control interface including the power supply input and the power
9 supply control output;
10 A memory control interface including the first clock; and
11 A control unit coupled to the system interface, the CLUT, the video
12 interface, the power control interface, the memory control interface, the 2D
13 engine and the 3D engine.

1 35. A graphics controller comprising:
2 A power supply input configured to receive power at a range of voltages;
3 A power supply control output;
4 A first clock;
5 A system power supply change input;
6 A first clock control output;
7 A second clock;
8 A second clock control output;
9 A brightness output configured to signal to a system that a reduction in
10 brightness of a display is appropriate;
11 A 2D engine;
12 A 3D engine;
13 A CLUT coupled to the 3D engine and coupled to the 2D engine;
14 A system interface including the system power supply input;
15 A video interface including the second clock and the second clock control
16 output;
17 A power control interface including the power supply input and the power
18 supply control output;
19 A memory control interface including the first clock; and
20 A control unit coupled to the system interface, the CLUT, the video
21 interface, the power control interface, the memory control interface, the 2D
22 engine and the 3D engine.

1 36. A method of managing power in a graphics controller, comprising:
2 Receiving a change indication related to a system power supply;
3 reducing a rate of a first clock;
4 reducing a controller power supply voltage;
5 Signaling a BIOS with an indication of a change related to the system
6 power supply;
7 Receiving a set of one or more available clock rates;
8 Checking a state of the graphics controller;
9 Choosing a desired clock rate from the set of available clock rates;
10 Adjusting a second clock to conform to the desired clock rate;
11 Disabling a first portion of circuitry responsive to checking the state of the
12 graphics controller.